

Attorney's Docket No.: 10559-391001
Client's Ref. No.: P10256 - ADI APD1812-1-US

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Number of pages including this page 21

FEB 22 2005

Applicant : Ryo Inoue et al.
Serial No. : 09/745,104
Filed : December 20, 2000

Art Unit : 2183
Examiner : Charles A. Harkness

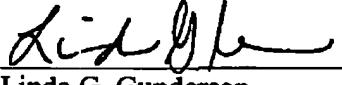
Title : Hardware Loops and A Pipeline System Using Advanced Generation of Loop
Parameters (As Amended)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attached to this facsimile communication cover sheet is a Response to Office Action,
faxed this 22nd day of February, 2005, to the United States Patent and Trademark Office.

Respectfully submitted,

Date: February 22, 2005



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Attorney's Docket No.: 10559/391001/P10256 - ADI APD1812-1-US
Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Ryo Inoue et al. Art Unit: 2183
Serial No.: 09/745,104 Examiner: Charles A. Harkness
Assignee : Intel Corporation
Analog Devices, Inc.
Filed : December 20, 2000
Title : HARDWARE LOOPS AND A PIPELINE SYSTEM USING ADVANCED
GENERATION OF LOOP PARAMETERS (AS AMENDED)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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AMENDMENT

In response to the Office action mailed November 19, 2004,
please amend the application as follows:

Amendments to the Claims begin on page 2 of this paper.

Remarks/Arguments begin on page 13 of this paper.

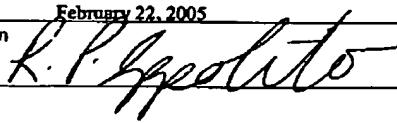
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I hereby certify that this correspondence is being transmitted by facsimile to the Patent and Trademark Office on the date indicated below.

Date of Transmission

February 22, 2005

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